A method for fabricating a semiconductor memory device is described. An insulating layer is disposed on a semiconductor substrate. A matrix of semiconductor memory elements is disposed in the substrate. The semiconductor memory elements include a plurality of contact holes formed in the insulating layer. One contact hole is formed in the insulating layer for each of the semiconductor memory elements. A bit definition region is disposed in the semiconductor substrate underneath each of the contact holes. A contact plug is disposed in each of the contact holes and is in electrical contact with the bit definition region. The bit definition region is configured such that a contact resistance between the semiconductor substrate and the contact plug defines a bit to be stored in the semiconductor memory elements. An evaluation circuit is connected to and evaluates the contact resistance of the semiconductor memory elements.

The paragraph starting on page 11, line 3 and ending on page 11, line 10 now reads as:

In all the figures of the drawing, sub-features and integral parts that correspond to one another bear the same reference symbol in each case. Referring now to the figures of the drawing in detail and first, particularly, to Fig. 1 thereof, there is shown a semiconductor memory device 1 formed of a substrate 10, an insulating layer 20 disposed on the substrate

A2 cancelled

10, contact holes 25 formed in the insulating layer 20, bit definition regions 30, and an implantation I_1 and an implantation I_2.

The paragraph starting on page 12, line 14 and ending on page 12, line 17 now reads as:

A3 ✓

All the contact holes 25 are defined and etched free photolithographically. The first implantation I_1 into a first group of the contact holes 25 is then performed using a dopant of the first conductivity type n.

The paragraph starting on page 12, line 19 and ending on page 12, line 21 now reads as:

A4 ✓

A second implantation I_2 is then performed using a dopant of a second conductivity type p in a second group of the contact holes 25.

The paragraph starting on page 13, line 1 and ending on page 13, line 3 now reads as:

A5 ✓

A third group of the contact holes 25 remains covered by masks 32 during both implantations, that is to say does not receive implantation.

The paragraph starting on page 13, line 5 and ending on page 13, line 9 now reads as:

A6 There are, then, the following semiconductor memory cells with increasing contact resistance: a contact implantation like the underlying substrate (e.g. like diffusion implantation), no implantation and contact implantation opposite to the underlying substrate.

The paragraph starting on page 13, line 20 and ending on page 13, line 21 now reads as:

A7 In Fig. 2, in addition to the reference symbols already introduced, contact plugs 40 are provided.

The paragraph starting on page 14, line 4 and ending on page 14, line 9 now reads as:

A8 The substrate 10 expediently has a strip-type conductor strip structure, e.g. polysilicon or diffusion strips, the strips each forming a second terminal of the memory cells on a top side of the substrate, which, in addition to the respective contact plug 40, forms a terminal 40' for an evaluation circuit with a resistance measuring device.